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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,347	02/06/2004	Toshihiro Sawamoto	9319S-000665	5263

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EXAMINER	
SOWARD, IDA M	

ART UNIT	PAPER NUMBER
2822	

MAIL DATE	DELIVERY MODE
03/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Supplemental Notice of Allowability	Application No.	Applicant(s)	
	10/774,347	SAWAMOTO ET AL.	
	Examiner	Art Unit	
	Ida M. Soward	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Printer Rush filed February 19, 2007*.

2. ☒ The allowed claim(s) is/are *1 and 4-13*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 01/24/2007
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

IDA M. SOWARD
PRIMARY EXAMINER

DETAILED ACTION

This Office Action is in response to the Printer Rush filed February 19, 2007.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Matthew Szalach on March 19, 2007.

The application has been amended as follows:

1. (Currently Amended) A semiconductor device, comprising:

a first semiconductor package in which a first semiconductor chip is mounted, the first semiconductor chip mounted on a top surface of a first carrier substrate of the first semiconductor package;

a second semiconductor package in which at least one semiconductor chip is mounted and is supported on the first semiconductor package such that ends of the second semiconductor package are arranged above the first semiconductor chip; and

a third semiconductor package that is supported on the first semiconductor package such that ends of the third semiconductor package are arranged above the first semiconductor chip;

wherein the second semiconductor package and the third semiconductor package are separated from each other.

2-3. (Cancelled)

4. (Previously Presented) The semiconductor device according to claim 1, wherein at least one of a size, thickness and material is different between the second semiconductor package and the third semiconductor package.

5. (Previously Presented) The semiconductor device according to claim 1, wherein at least one gap selected from the group including:

a gap between the second semiconductor package and the third semiconductor package;

a gap between the first semiconductor package and the second semiconductor package; and

a gap between the first semiconductor package and the third semiconductor package;

is filled with resin.

6. (Currently Amended) The semiconductor device according to claim 1, wherein:

~~the first semiconductor package further comprises:~~

~~a first carrier substrate in which a~~ the first semiconductor chip is flip-chip mounted on the first carrier substrate; ~~and~~

~~the second semiconductor package further comprises:~~

~~a~~the second semiconductor chip~~;~~ is mounted on a second carrier substrate ~~in which the second semiconductor chip is mounted~~;

protruding electrodes ~~which~~ are bonded onto the first carrier substrate and ~~holds~~ hold the second carrier substrate above the first semiconductor chip; and

a sealing agent, which seals the second semiconductor chip.

7. (Original) The semiconductor device according to claim 6, wherein the first semiconductor packages is a ball grid array in which the first semiconductor chip is flip-chip mounted on the first carrier package, and the second semiconductor package is one of a ball grid array and a chip-size package in which the second semiconductor chip mounted on the second carrier substrate is sealed with a mold.

8. (Original) The semiconductor device according to claim 6, wherein the protruding electrodes are arranged at least at four corners of the second carrier substrate, and are excluded from a mounting region of the first semiconductor chip.

9. (Original) The semiconductor device according to claim 6, wherein the first semiconductor chip is a logic-processing element, and the second semiconductor chip is a memory element.

10. (Currently Amended) A semiconductor device, comprising:

a first semiconductor package in which a first semiconductor chip is mounted, the first semiconductor chip mounted on a top surface of a first carrier substrate of the first semiconductor package;

a second semiconductor package having a second semiconductor chip that is supported on the first semiconductor package such that ends of the second semiconductor chip are arranged above the first semiconductor chip; and

a third semiconductor package having a third semiconductor chip that is supported on the first semiconductor package such that ends of the third semiconductor chip are arranged above the first semiconductor chip;

wherein the second semiconductor package and the third semiconductor package are separated from each other.

11. (Original) The semiconductor device according to claim 10, wherein the second semiconductor chip includes a three-dimensional mounting structure.

12. (Currently Amended) An electronic device, comprising:

a first package in which an electronic component is mounted on a top surface of a first carrier substrate of the first semiconductor package;

a second package that is supported on the first package such that ends of the second package are arranged above the electronic component; and

a third package that is supported on the first package such that ends of the third package are arranged above the electronic component;

wherein the second package and the third package are separated from each other.

13. (Currently Amended) Electronic equipment, comprising:

a first semiconductor package in which a semiconductor chip is mounted on a top surface of a first carrier substrate of the first semiconductor package;

a second semiconductor package that is supported on the first semiconductor package such that ends of the second semiconductor package are arranged above the semiconductor chip;

a motherboard on which the second semiconductor package is mounted; and

a third semiconductor package that is supported on the first semiconductor package such that ends of the third semiconductor package are arranged above the semiconductor chip;

wherein the second semiconductor package and the third semiconductor package are separated from each other.

14-18. (Cancelled)

Allowable Subject Matter

Claims 1 and 4-13 are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to semiconductor devices:

Chee et al. (US 2003/0089977 A1)

Kim (6,121,682)

Matsuo et al. (US 6,717,251 B2)

Pu et al. (US 6,610,259 B2)

Sakiyama et al. (US 6,914,259 B2)

Shibata (US 6,727,582 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IMS
March 22, 2007

IDA M. SOWARD
PRIMARY EXAMINER